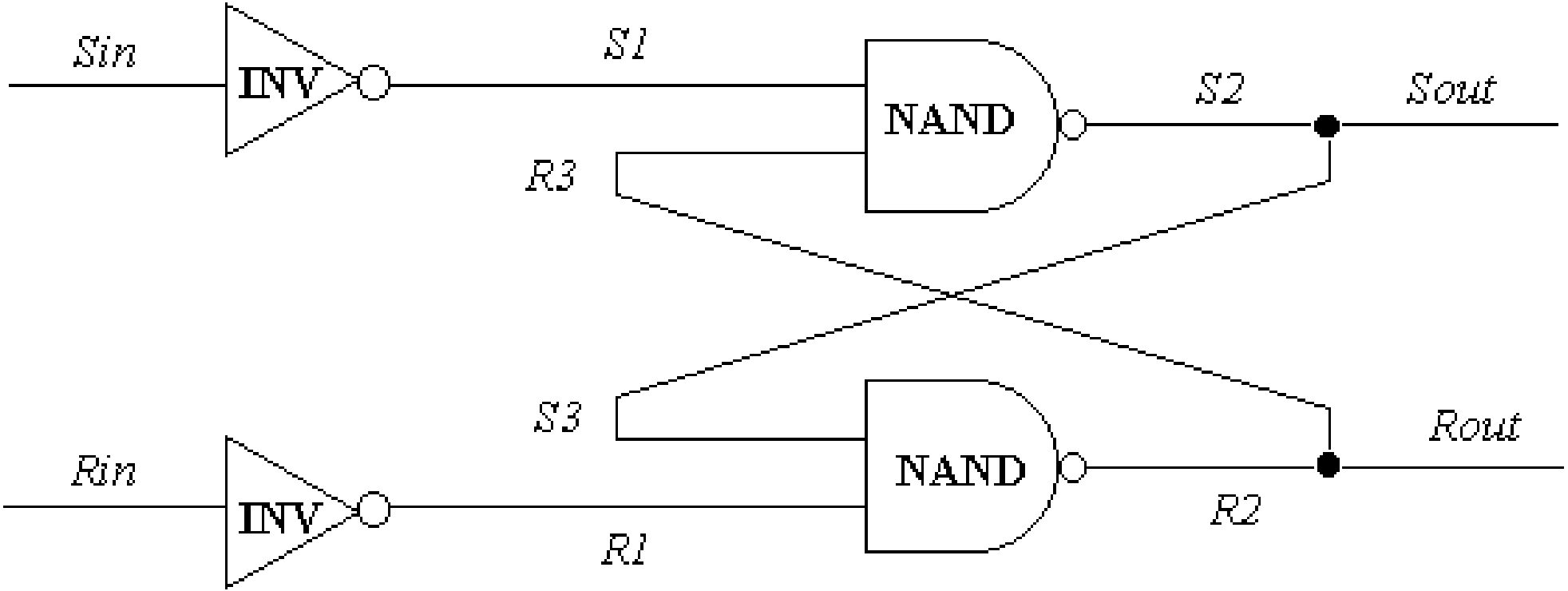
Sin
INV
S1
NAND
S2
Sout
R3
S3
NAND
Rout
Rin
INV
R1
R2